

## WHAT IS CLAIMED IS:

1           1.    An MPEG decoder comprising:

2                   a packetized elementary stream (PES) interface capable of  
3 receiving a plurality of packetized elementary streams associated  
4 with a single video program;

5                   a presentation time stamp (PTS) detection circuit capable  
6 of detecting presentation time stamps in said packetized elementary  
7 streams and extracting said presentation time stamps therefrom; and

8                   a selection circuit capable of selecting presentation  
9 time stamps associated with a first one of said plurality of  
10 packetized elementary streams and transmitting said selected  
11 presentation time stamps to a clock generation circuit, wherein  
12 said clock generation circuit generates a first reference clock  
13 signal used by a first decoder to decode said first packetized  
14 elementary stream.

1           2.    The MPEG decoder as set forth in Claim 1 wherein said  
2 clock generation circuit further generates a second reference clock  
3 signal synchronized to said first reference clock signal and  
4 wherein said second reference clock signal is used by a second  
5 decoder to decode a second packetized elementary stream in  
6 synchronization with said first packetized elementary stream.

1           3.    The MPEG decoder as set forth in Claim 2 wherein said  
2   selected presentation time stamps are video presentation times  
3   stamps and said first decoder is a video decoder.

1           4.    The MPEG decoder as set forth in Claim 3 wherein said  
2   second decoder is an audio decoder.

1           5.    The MPEG decoder as set forth in Claim 2 wherein said  
2   selected presentation time stamps are audio presentation times  
3   stamps and said first decoder is an audio decoder.

1           6.    The MPEG decoder as set forth in Claim 5 wherein said  
2   second decoder is a video decoder.

1           7.    The MPEG decoder as set forth in Claim 2 said clock  
2   generation circuit generates said second reference clock signal by  
3   synchronizing presentation time stamps associated with said second  
4   packetized elementary stream with said selected presentation time  
5   stamps associated with said first packetized elementary stream.

1           8. A digital video recorder capable of playing back a  
2 recorded television program stored as packetized elementary  
3 streams, said digital video recorder comprising:

4           a video processor capable of receiving an incoming  
5 television program and converting said incoming television program  
6 to a baseband video signal capable of being displayed on a  
7 television set coupled to said digital video recorder;

8           a storage disk capable of storing said incoming  
9 television program as packetized elementary streams during  
10 recording; and

11          an MPEG decoder comprising:

12           a packetized elementary stream (PES) interface  
13 capable of receiving a plurality of packetized elementary  
14 streams associated with said recorded television program from  
15 said storage disk during playback;

16           a presentation time stamp (PTS) detection circuit  
17 capable of detecting presentation time stamps in said  
18 packetized elementary streams and extracting said presentation  
19 time stamps therefrom; and

20           a selection circuit capable of selecting  
21 presentation time stamps associated with a first one of said  
22 plurality of packetized elementary streams and transmitting

23        said selected presentation time stamps to a clock generation  
24        circuit, wherein said clock generation circuit generates a  
25        first reference clock signal used by a first decoder to decode  
26        said first packetized elementary stream.

1        9.    The digital video recorder as set forth in Claim 8  
2        wherein said clock generation circuit further generates a second  
3        reference clock signal synchronized to said first reference clock  
4        signal and wherein said second reference clock signal is used by a  
5        second decoder to decode a second packetized elementary stream in  
6        synchronization with said first packetized elementary stream.

1        10.   The digital video recorder as set forth in Claim 9  
2        wherein said selected presentation time stamps are video  
3        presentation times stamps and said first decoder is a video  
4        decoder.

1        11.   The digital video recorder as set forth in Claim 10  
2        wherein said second decoder is an audio decoder.

1           12. The digital video recorder as set forth in Claim 9  
2 wherein said selected presentation time stamps are audio  
3 presentation times stamps and said first decoder is an audio  
4 decoder.

1           13. The digital video recorder as set forth in Claim 12  
2 wherein said second decoder is a video decoder.

1           14. The digital video recorder as set forth in Claim 9 said  
2 clock generation circuit generates said second reference clock  
3 signal by synchronizing presentation time stamps associated with  
4 said second packetized elementary stream with said selected  
5 presentation time stamps associated with said first packetized  
6 elementary stream.

1           15. For use in a digital video recorder, a method for  
2 decoding a television program stored in MPEG format:

3           receiving in an MPEG decoder a plurality of packetized  
4 elementary streams associated with the stored television program;

5           detecting presentation time stamps in the packetized  
6 elementary streams;

7           extracting the presentation time stamps from the  
8 packetized elementary streams;

9           selecting presentation time stamps associated with a  
10 first one of the plurality of packetized elementary streams; and

11           generating from the selected presentation time stamps a  
12 first reference clock signal used by a first decoder to decode the  
13 first packetized elementary stream.

14           16. The method as set forth in Claim 15 further comprising  
2 the step of generating a second reference clock signal synchronized  
3 to the first reference clock signal, wherein the second reference  
4 clock signal is used by a second decoder to decode a second  
5 packetized elementary stream in synchronization with the first  
6 packetized elementary stream.

1           17. The method as set forth in Claim 14 wherein the selected  
2 presentation time stamps are video presentation times stamps and  
3 the first decoder is a video decoder.

1           18. The method as set forth in Claim 17 wherein the second  
2 decoder is an audio decoder.

1           19. The method as set forth in Claim 16 wherein the selected  
2 presentation time stamps are audio presentation times stamps and  
3 the first decoder is an audio decoder.

1           20. The method as set forth in Claim 19 wherein the second  
2 decoder is a video decoder.

1           21. The method as set forth in Claim 16 wherein the step of  
2 generating a second reference clock signal comprises the sub-step  
3 of synchronizing presentation time stamps associated with the  
4 second packetized elementary stream with the selected presentation  
5 time stamps associated with the first packetized elementary stream.